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#10 Green 3/20/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Xiaowei Deng	Docket No:	TI-29320
Serial No:	09/932,763	Conf. No:	5414
Examiner:	Daniel D. Chang	Art Unit:	2818
Filed:	08/16/2001		
For:	SILICON-ON-INSULATOR DYNAMIC LOGIC		

APPEAL BRIEF UNDER 37 C.F.R. 1.192

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that this Appeal Brief filed, in triplicate, under 37 CFR 1.192 is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, DC 20231 on 3-12-03.

Ann Trent
Ann Trent

Assistant Commissioner of Patents
Washington, D. C. 20231

Dear Sir:

The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the final rejection mailed October 16, 2002, and the Advisory Action mailed January 9, 2003.

Real Party in Interest under 37 C.F.R. 1.192(c)(1)

Texas Instruments Incorporated is the real party in interest.

Related Appeals and Interferences under 37 C.F.R. 1.192 (c)(2)

There are no related appeals or interferences known to appellant, the appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the board's decision in the pending appeal.

Status of Claims on Appeal under 37 C.F.R. 1.192 (c)(3)

Claims 1-3, 5-7, 9-11, and 13-15 were rejected. Claims 4, 8, 12, and 16 were objected to. Claims 1-16 are pending in this case. Claims 1-16 are appealed.

Status of Amendments Filed After Final rejection under 37 C.F.R. 1.192 (c)(4)

The amendment filed by the applicant on 12/02/2002 was not entered by the examiner.

Summary of the Invention under 37 C.F.R. 1.192(c)(5)

The invention is a dynamic logic circuit on a SOI substrate. The circuit comprises a pull-down network comprising a plurality of series connect MOS transistors where at least one the series connected transistors is a NMOS transistor and at least one is a PMOS transistor. The dynamic logic circuit also comprises a precharge circuit connected to a clock signal, the circuit supply voltage and the pull-down network. A ground switch circuit is connected to the clock signal and to the pull-down network, and the output node is taken from the common node of the pull-down network and the precharge circuit. Other embodiments of the instant invention include a pull-down network of series connected PMOS transistors, a pull-down network of a plurality of parallel connected transistors with at least one PMOS transistor and one NMOS transistors, and a pull-down network of parallel connected PMOS transistors.

Statement of Issues Presented for Review under 37 C.F.R. 1.192 (C)(6)

1. Are claims 1-3, 5-7, 9-11, and 13-15 properly rejected under 35 U.S.C. 102(e) as being anticipated by the Hagihara patent (US2001/0001229A1).

2. Are claims 4, 8, 12, and 16 properly objected to.

Statement of the Grouping of Claims under 37 C.F.R. 1.192(C)(7)

Claims 1-16 stand or fall together.

Arguments

1. Are claims 1-3, 5-7, 9-11, and 13-15 properly rejected under 35 U.S.C. 102(e) as being anticipated by the Hagihara patent (US2001/0001229A1).

Appellants respectfully submit that claims 1-3, 5-7, 9-11, and 13-15 are not properly rejected under 35 U.S.C. 102(e) as being anticipated by the Hagihara patent.

In his response on October 11, 2002 the examiner states that the Hagihara patent discloses a pull-down network in Figure 1 and also in paragraph [0005]. In addition to stating that a reference numeral 10 shows a logic circuit, paragraph [0005] also states that the logic circuit consists of n-type or p-type MOS transistors or both n-type and p-type MOS transistors. The examiner further states, "figure 1 does not specifically show the connections of n-type or p-type MOS transistors. It only shows a LOGIC CIRCUIT box with a reference numeral 10." The examiner is exactly correct in his interpretation of the Hagihara patent. It does not specifically show the connections of n-type or p-type MOS transistors, it only shows a logic circuit box with a reference numeral 10. The examiner then argues that the limitations of all the claims 1-3, 5-7, 9-11, and 13-15 are inherent in the Hagihara patent.

The standard for inherency can be found in Continental Can Company USA, Inc. v. Monsanto Company, 948 F.2d 1264; 1991 U.S. App. LEXIS 26994; 20 U.S.P.Q.2D (BNA) 1746, and followed in Rockwell International Corporation and Rockwell Science Center, Inc., vs SDL, Inc, 103 F.Supp.2d 1202; 2000 U.S. Dist. LEXIS 9247. In Continental the Court states:

To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing description matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.

Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing *may* result from a given set of circumstances is not sufficient. If, however, the disclosure is sufficient to show the natural result flowing from the operation as taught would result in the performance of the questioned function, it seems to be well settled that the disclosure should be regarded as sufficient.

In the language of the Court, inherency may **not** be established by **probabilities** or **possibilities**. The examiner has already stated that all the Hagihara patent shows is a box labeled LOGIC CIRCUIT. Now while the examiner may speculate as to what could possibly be contained in the box, or what may probably be in the box, there is nothing in the Hahihara patent that would lead one to a natural result that describes the limitations of any of the claims of the instant invention as required by the Court. Therefore under the current interpretation of inherency claims 1-3, 5-7, 9-11, and 13-15 are not properly rejected under 35 U.S.C. 102(e) as being anticipated by the Hagihara patent (US2001/0001229A1).

2. Are claims 4, 8, 12, and 16 properly objected to.

In amending the claims 4, 8, 12, and 16 in the action dated 12-10-2002, the appellants included the limitations of base claims and any intervening claims as requested by the examiner in an action dated 10-11-2002. The examiner refused to enter the amended claims. Appellants argue that the amended claims comply with the requirements of the examiner and should have been entered. Furthermore claims 4, 8, 12, and 16 all depend

from independent claims 1, 5, 9, and 13 respectively. Is has been shown previously that independent claims 1, 5, 9, and 13 are allowable over the Hagihara patent. Dependent claims 4, 8, 12, and 16 all contain the limitations of the independent claims and are also allowable over the cited art. Allowable claims 4, 8, 12, and 16 were therefore improperly objected to.

Conclusion

For the foregoing reasons, Appellant respectfully submits that the Examiner's final rejection of Claims 1-16 under 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,

Peter McLarty
Reg. No. 44,923
Attorney for Appellant

Texas Instruments Incorporated
P. O. Box 655474, MS 3999
Dallas, Texas 75265
(972) 917-4258